PRODUCTION TECHNOLOGY DEVELOPMENT FOR HIGH YIELD, HIGH PERFORMANCE X-BAND MONOLITHIC POWER AND LOW NOISE AMPLIFIERS

C.D. Chang, S.K. Wang, L.C.T. Liu, M. Siracusa,
H. Yamasaki, and J.M. Schellenberg

Hughes Aircraft Company
Torrance Research Center
3110 W. Lomita Boulevard, Torrance, CA 90509

ABSTRACT

A production technology for high yield and high performance MMICs has been developed. Two stage X-band power amplifier and low noise amplifiers were used as test vehicles in this producibility study. The power amplifier chips have consistently demonstrated a 1.5 watt output power with 9 dB gain and 20% power added efficiency. The low noise amplifier chips have achieved a reproducible performance of less than 3 dB noise figure with 20 dB gain. Producibility improvement of MMIC chip fabrication has achieved an average yield well in excess of 10%.

INTRODUCTION

In recent years, Producibility of GaAs monolithic microwave integrated circuits (MMICs) has become a real possibility due to the advancements in material and wafer processing technology. A number of laboratories have produced monolithic circuits with state-of-the-art performance[1]-[4]. Yet to date, only a few of them have addressed the issues of the producibility. At Hughes Torrance Research Center, a production technology for high-yield, high performance MMIC has been developed. It combines the optimum material and processing techniques as well as the monolithic circuit design consideration. In this study, a two stage monolithic power amplifier and a two-stage low noise amplifier have been developed, produced, and tested. This effort is to demonstrate the feasibility of manufacturing these cost effective, reproducible amplifier chips.

In this paper, details of both monolithic power amplifiers and low noise amplifier will be presented. The amplifier circuit design, material and processing improvement will be discussed and the performance results of both amplifiers will be shown. Finally the yield data of this study will be discussed.

MONOLITHIC CIRCUIT DESIGN

Power Amplifier

The base line approach for the monolithic power amplifier circuit design employs a single-ended, two stage configuration. A 1500 μm X 0.8 μm FET was used for the driver stage and a 3600 μm X 0.8 μm FET which consisted of two 1800 μm gate width FETs, were used for the output stage. In order to have the capability of biasing from both sides of amplifier chips, the amplifier chip has a symmetrical circuit design. Figure 1 shows the schematic circuit design for the power amplifier. S-parameter data were measured from discrete FETs; an in-house optimization program was used to generate the FET equivalent circuit model from the measured data.

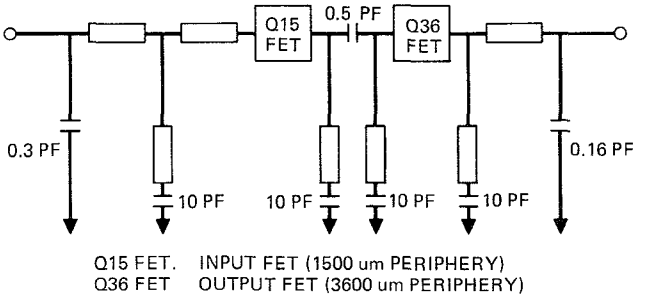

Figure 1. Two Stage Power Amplifier Design.

The output matching network was synthesized to obtain the maximum power output, while the input and interstage networks were designed to provide the gain flatness. The interdigitated capacitors were used as the RF matching elements while the overlay metal-oxide-metal capacitors were used as the DC blocking capacitors. After the matching networks were synthesized, SUPER-COMPACT simulation program was used to optimize the final matching networks which consisted of all the microstrip transmission lines, discontinuities and other monolithic passive components. The photo of a finished monolithic power amplifier is shown in Figure 2. There are thirty-four 0.8 μm gate fingers, eight 10 pf overlay capacitors, twenty-seven airbridges and eleven via holes on each chip. The chip size of the power amplifier is 1.94 mm X 3.0 mm.

Low Noise Amplifier

A single-ended and two-stage approach was chosen for the monolithic low noise amplifier. Microstrip transmission lines were used for RF matching because of their low-loss, low dispersion and useful impedance range. The amplifiers used two 0.5 X 300 μm gate FETs. The FET equivalent circuit model was generated from the measured data of discrete FETs. An in-house program was then used to calculate the optimized noise model. The input matching network was synthesized to provide the calculated optimum source impedance for the FET to obtain the lowest noise figure, while the interstage and output matching circuits were designed to provide the gain match. The circuit schematics for the low noise amplifier is shown in Figure 3. MOM overlay capacitors were used for RF

CH2191-5/85/0000-0046 $1.00 © 1985 IEEE

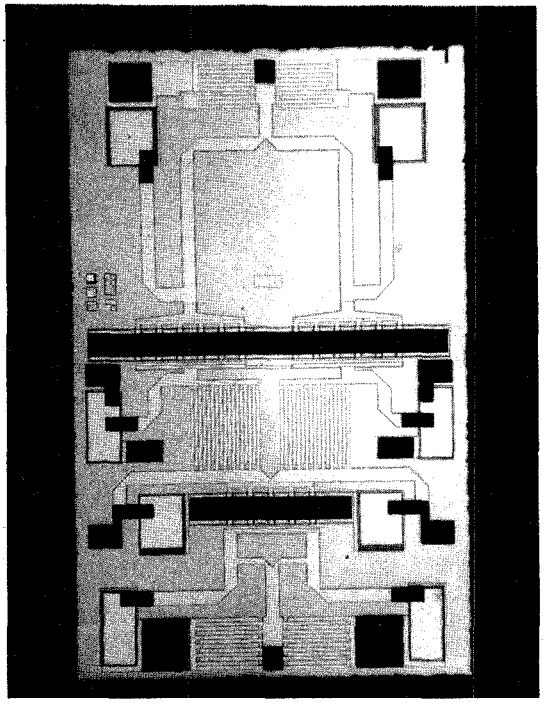

Figure 2. X-Band 2-Stage Monolithic Power Amplifier.

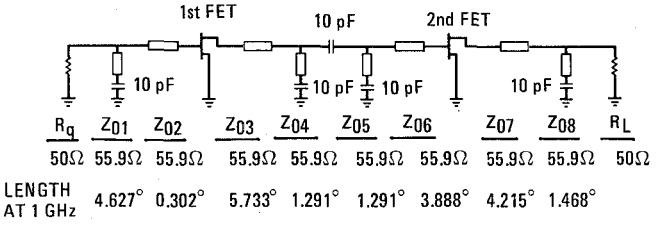

Figure 3. LNA Design.

bypassing and blocking applications. Airbridges were employed to interconnect the FET source pads and to connect the microstrip line to the top plate of the overlay capacitors. A substrate thickness of 0.1 mm was chosen to facilitate the fabrication of via hole with high yield. The use of the via hole ground allowed greater flexibility in the layout of the amplifier because grounds can be placed almost anywhere on a circuit rather than only at the substrate edges. In addition, it could lower the source grounding inductance and reduce the time required to mount the amplifier circuit. The gates and drains of both stage FETs were connected together through high impedance microstrip lines to simplify the bias circuitries. Figure 4 shows a photo of the finished low noise amplifier chip. There are eight 0.5 μm gate fingers, five 10 pf overlay capacitors, eleven airbridges and five via holes on each amplifier chip.

MATERIAL AND PROCESSING IMPROVEMENTS

A block diagram of the MMIC fabrication procedure is given in Figure 5. The critical steps that affect the MMIC performance and yield have been identified as

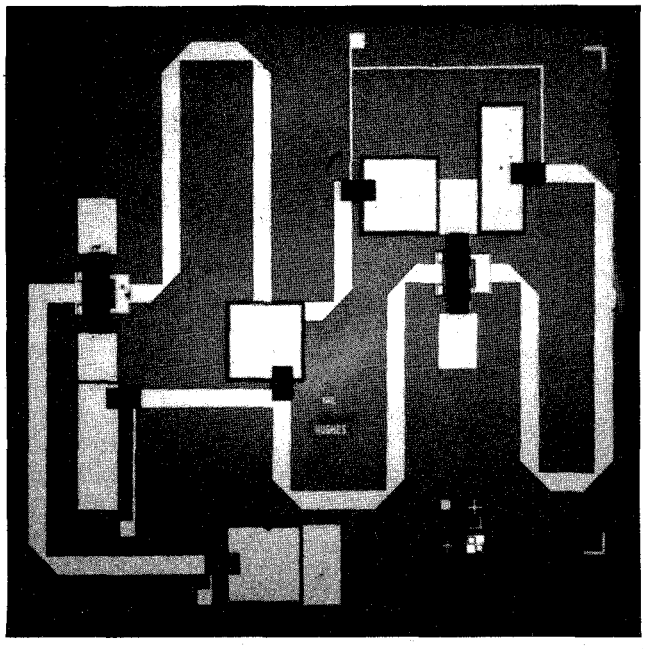

Figure 4. X-Band 2-Stage Monolithic Low Noise Amplifier.

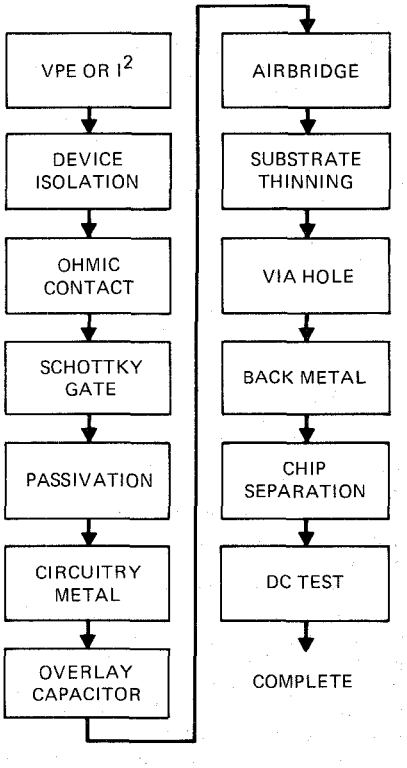

Figure 5. Block Diagram of Fabrication Procedure.

materials, gates, passivation, overlay capacitors, airbridges and via holes.

Various GaAs materials including doped VPE, ion implantation into buffer layer and direct implantation into semi-insulating GaAs substrates, have been evaluated for

both amplifiers. The selection criteria were: circuit performance, uniformity and reproducibility and cost effectiveness. Although direct implantation has the advantages of lower cost and better on wafer uniformity, VPE material were selected for this producibility study because of the better circuit performance and consistency from wafer to wafer.

The gate process includes definition by photolithography, recess etching and metallization. We are able to define the 0.8 μm long gates for power amplifier and 0.5 μm long gates for the low noise amplifier with about 50% yield using an improved contact photolithography. Ti/Pt/Au and Aluminum gate metallizations are used in power and low noise amplifiers respectively, for optimum chip yield and circuit performance.

MMIC passivation is done by depositing 2000Å of CVD SiO_2 film on the FET channel surface. In terms of power, gain and noise figure, passivation has little effects on the circuit performance, but the frequency response shifts down by 500 MHz due to the changes in the FET characteristics. This frequency shift, however, is not a problem as long as it is taken into account in the overall circuit design. Amplifier chips with SiO_2 passivation have passed an environment test at 135°C and 30 PSI.

MOM overlay capacitors are formed by sputtering a 2500Å dielectric SiO_2 film over the bottom metal layer. The major cause of overlay capacitor failure was identified as pinholes in the dielectric film. Stringent wafer cleaning and handling steps, implemented to eliminate the causes for pinholes, have resulted in better than 95% yield for an 10 pf capacitor.

Airbridge process has been improved to eliminate problems of photo resist cracking, gold underplating and thickness control. The size and uniformity of via holes are very sensitive to the exact wafer thickness and parallelism after wafer thinning down to the nominal 100 μm design values. Using a combination of improved lapping technique and chem-mechanical polishing, GaAs wafer can be thinned down to 100 $\pm$5 μm with a mirror finish and damage-free surface, which in turn results in a high yield for wet-chemically etched via holes.

AMPLIFIER YIELD

More than seventy 2-inch GaAs wafers have been processed for both MMIC chips in a period of six months. Chip yield data have been accumulated and analyzed. For the power amplifier, the yield for the two FETs with 5.1 mm total gate width is about 45%, the yield for the microstrip transmission lines and interdigital capacitors is about 95%, the yield for eight overlay capacitors is about 60%, the yield for airbridges is abour 95% and the yield for via holes is about 90%. In addition, about 10% of the chips are lost due to handling, edge effect and dicing, and about 20% of the chips are rejected because the DC parameters (I_{DSS} and V_{po}) fall outside of the acceptance windows determined by DC-RF correlation. The best DC yield achieved from a single 2-inch diameter wafer is 33%. This high chip yield was accomplished by identifying and improving the critical fabrication steps through processing a large number of wafers. Even higher chip yield is expected when we continue on the learnng curve for MMIC production.

CIRCUIT PERFORMANCE

In the monolithic power amplifier, sample chips from each process wafer lot have been mounted in the test fixtures and RF tested. An automatic network analyzer system was used to measure the S-parameters of the amplifier chips. The typical small signal gain of the power amplifier is about 11 dB at 9.5 GHz. Output power from many amplifier chips was measured and a typical output power of 1.5 Watt with 9 dB associated gain with 20% power added efficiency has been achieved. The best output power of 2 Watt with 8.5 dB gain at 9.5 GHz has also been demonstrated. Output power curves of 38 power amplifier chips from 12 different wafers are shown in Figure 6. The output power distribution of these amplifier chips are also shown in Figure 7. The phase tracking variation was approximately 7 degrees from chip to chip in the same wafer and was approximately 18 degrees from wafer to wafer.

Sample low noise amplifier chips were measured and the gain-noise figure of ten amplifiers from four different wafers are shown in Figure 8. A typical associated gain of over 20 dB with better than 3 dB noise figure across the 1 GHz bandwidth has been achieved.

CONCLUSION

Combining the choice of optimum material, refined processing techniques and relaxing the constraints of circuit design, a MMIC production technology for high yield, high performance circuits have been developed. Producibility improvement of MMIC chip fabrication achieved an average yield well in excess of 10% for two stage X-band power amplifier delivering 1.5 watt output

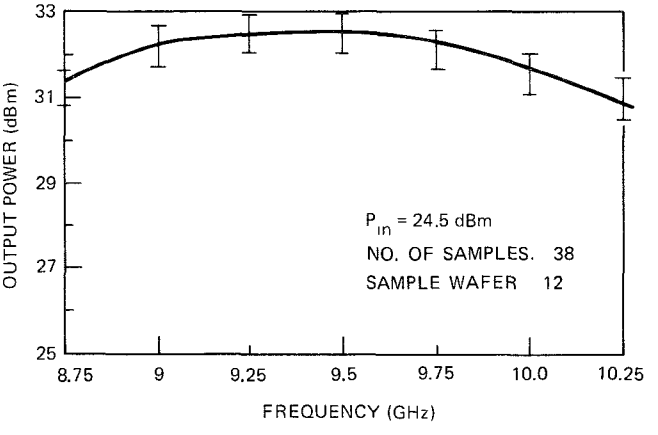

Figure 6. Frequency Response of Output Power for Power Amplifier.

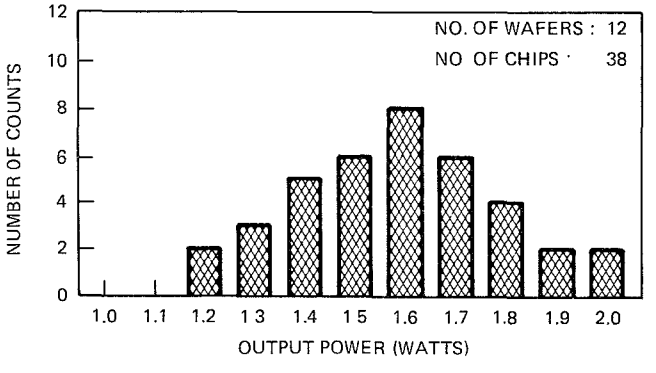

Figure 7. Distribution of Output Power.

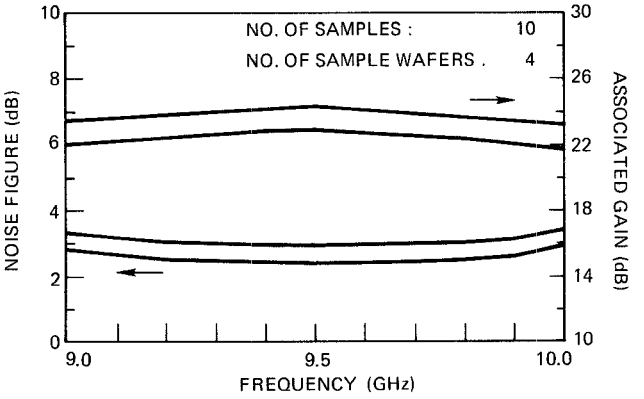

Figure 8. Gain and Noise Figure of LNA.

power with 9 dB gain and 20% power added efficiency and two stage X-band low noise amplifier yielding less than 3 dB noise figure with 20 dB gain.

This work has demonstrated an excellent yield of large MMIC chips. Based on this experience we believed that future refinement of design and processing will improve the yield to 25% or larger, and then it will result in low cost MMIC chips. With a DC chip yield of 30% or higher, the cost goal of the amplifier chips will be as low as $20 per chip in the future for the mass production.

ACKNOWLEDGEMENT

The authors would like to thank R. Tang, R. Burns for their support; also thanks to Dr. H.J. Kuno for his continuing support and encouragement. We would like to acknowledge the effort by R. Pauley, P. Asher, P. Busted, L. Marich, S. Rodriquez, M. Neveux and D. Hynds.

REFERENCES

1. Y. Ayasli, et al, "Capacitively Coupled Traveling-Wave Power Amplifier," 1984 IEEE Microwave and Millimeter-Wave Monolithic Circuit Symposium, Digest of Papers, p. 52, May 1984.

2. D. Maki, et al, "A 69 GHz Monolithic FET Oscillator," 1984 IEEE Microwave and Millimeter-Wave Monolithic Circuit Symposium, Digest of Papers, p. 62, May 1984.

3. A.M. Pavio, et al, "A Monolithic Multi-Stage 6-18 GHz Feedback Amplifier," 1984 IEEE Microwave and Millimeter-Wave Monolithic Circuit Symposium, Digest of papers, p. 45, May 1984.

4. L.C.T. Liu, D.W. Maki, C. Storment, M. Sokolich and W. Klatskin, "An 8-18 GHz Monolithic Two-Stage Low Noise Amplifier," Digest of IEEE 1984 Microwave and Millimeter-Wave Monolithic Circuits Symposium, pp. 49-51, May 1984.